WHAT IS CLAIMED IS:

1. A semiconductor device having a semiconductor substrate formed with a plurality of electrode pads, and wiring electrically connecting said electrode pads to external electrodes to be connected to conductive patterns formed on an external circuit board, said wiring formed in a plurality of layers, said semiconductor device comprising:

insulating layers interposed between the layers of said wiring, and between the lowermost layer of said wiring and said semiconductor substrate, thereby to ensure insulation therebetween;

said layers of said wiring each having depressed portions located at via holes formed in said insulating layers, said depressed portions connected to the lower layer of said wiring or said electrode pads;

bump electrodes formed on said depressed portions of the uppermost layer of said wiring;

external electrodes formed on the top surfaces of said bump electrodes; and

a sealing layer formed over said uppermost layer of said wiring so as to expose the top surface of said bump electrodes.

2. A semiconductor device according to claim 1, wherein said depressed portions of said layers of said wiring including said uppermost layer are formed in positions where said depressed portions overlap with each other.

3. A semiconductor device according to claim 1, wherein each of said bump electrodes is formed so as to erect from a bottom portion of the corresponding depressed portion.

4. A semiconductor device according to claim 1, wherein each of said bump electrodes is formed so as to cover the corresponding depressed portion.

5. A semiconductor device according to claim 1, wherein an uppermost insulating layer is further formed between said sealing layer and said uppermost layer of said wiring, said uppermost insulating layer having a substantially flat surface and does not include a filler material.

6. A semiconductor device according to claim 1, further comprising seed layers each formed under the corresponding layer of said wiring and acting as an electrode for forming the corresponding layer of said wiring.

7. A semiconductor device according to claim 6, wherein said seed layer has opening at each of said depressed portions of said wiring.

8. A semiconductor device according to claim 6, wherein said seed layers except the seed layer formed under said lowermost layer of said wiring are made of a material that is the same as that of said wiring.

9. A semiconductor device according to claim 1, wherein each of said external electrodes is made of a solder material including tin, each of said bump electrodes is made of copper, and a barrier layer including nickel is formed between each of said external electrodes and the corresponding bump electrode.

10. A semiconductor device according to claim 1, wherein, assuming that distances from a neutral point of a thermal stress of the semiconductor device to an arbitrary pair of bump electrodes among said bump electrodes are set as L_1 and L_2, and heights of said pair of bump electrodes are set as H_1 and H_2, the heights of said pair of bump electrodes are determined so as to satisfy:

when $L_1<L_2$, then $H_1 \leq H_2$.

11. A semiconductor device comprising:

a semiconductor substrate which has a main surface;

an electrode pad which is formed on the main surface;

a plurality of redistribution wirings which are formed over the main surface and which are formed at different levels, wherein the redistribution wiring at lowermost level is connected to the electrode pad and wherein the redistribution wiring at uppermost level has a depressed portion to which the redistribution wiring at lower level is connected;

a bump electrode which is formed on the depressed portion of the redistribution wiring at uppermost level;

an external electrode which is formed on the top surface of the bump electrode; and

a sealing layer which is formed over the redistribution wiring at uppermost level so as to expose the top surface of the bump electrode.

12. A semiconductor device according to claim 11, wherein the redistribution wiring at lower level has a depressed portion and wherein the depressed portion of the redistribution wiring at uppermost level and the depressed portion of the redistribution wiring at lower level are positioned to overlap each other.

13. A semiconductor device according to claim 11, wherein the bump electrode is formed so as to erect from a bottom portion of the depressed portion.

14. A semiconductor device according to claim 11, wherein the bump electrode is formed so as to cover the depressed portion entirely.

15. A semiconductor device according to claim 11, further comprising an insulating layer which is formed between the sealing layer and the redistribution wiring at uppermost level and which has a substantially flat

surface and does not include a filler material.

16. A semiconductor device comprising:

a semiconductor substrate which has a main surface;

a plurality of electrode pads which are formed on the main surface;

a plurality of redistribution wirings which are formed over the main surface and which are formed at different levels, wherein the redistribution wirings at lowermost level are connected to corresponding electrode pads and the redistribution wirings at uppermost level are coupled to corresponding redistribution wirings at lowermost levels through redistribution wirings at middle level;

a plurality of bump electrodes which are formed on corresponding portions of the redistribution wirings at uppermost level;

a plurality of external electrodes which are formed on the top surface of corresponding bump electrodes; and

a sealing layer which is formed over the redistribution wirings at uppermost levels so as to expose the top surface of the bump electrodes,

wherein assuming that distances from a neutral point of a thermal stress of the semiconductor device to an arbitrary pair of bump electrodes among the bump electrodes are set as L_1 and L_2, and length of the pair of bump electrodes are set as H_1 and H_2, the length of the pair of bump electrodes are determined so as to satisfy:

when $L_1<L_2$, then $H_1 \leq H_2$.

17. A semiconductor device comprising:

a semiconductor substrate which has a main surface;

an electrode pad which is formed on the main surface;

a plurality of insulating layers which are formed over the main surface, which are formed at different levels and which have via holes;

a plurality of redistribution wirings which are formed at different levels, the redistribution wiring at each level being formed on a surface and

the via hole of corresponding insulating layer, wherein the redistribution wiring at lowermost level is connected to the electrode pad and wherein the redistribution wiring at uppermost level has depressed portion located at the via hole defined by the insulating layer at uppermost level and connected to the redistribution wiring of lower level at the via hole;

a bump electrode which is formed on the depressed portion of the redistribution wiring at uppermost level;

an external electrode which is formed on the top surface of the bump electrode; and

a sealing layer which is formed over the redistribution wiring at uppermost level so as to expose the top surface of the bump electrode.

18. A semiconductor device according to claim 17, wherein the redistribution wiring at lower level has a depressed portion located at the via hole of the insulating layer at the lower level and wherein the via hole of the insulating layer at uppermost level and the via hole of the insulating layer at lower level are positioned to overlap each other.

19. A semiconductor device according to claim 17, wherein the bump electrode is formed so as to erect from a bottom of the via hole.

20. A semiconductor device according to claim 17, wherein the bump electrode is formed so as to cover the via hole entirely.